

WHAT IS CLAIMED IS:

1. A memory device comprising:  
a memory unit; and  
an arbiter controlling said memory unit while arbitrating for bus  
access requests from a plurality of units, wherein  
5 when a second bus access request takes place before an access to said  
memory unit that corresponds to a first bus access request has been  
completed, said arbiter performs activation of said memory unit that  
corresponds to said second bus access request in parallel with the access to  
said memory unit that corresponds to said first bus access request.
2. The memory unit according to claim 1, wherein  
said arbiter outputs an acknowledge signal that corresponds to said  
second bus access request before the access to said memory unit that  
corresponds to said first bus access request has been completed.
3. The memory device according to claim 1, wherein  
said memory unit has a plurality of memory banks, and  
said arbiter has a plurality of address ports corresponding to said  
plurality of units, and outputs an address corresponding to said second bus  
5 access request to said memory unit in parallel with an access to a first  
memory bank within said memory unit that corresponds to said first bus  
access request to activate a second memory bank different from said first  
memory bank.
4. The memory device according to claim 1, wherein  
said memory device contains said plurality of units.